Reg. No. ☐☐☐☐☐☐☐☐☐☐

ELH 402

First Semester M.Sc. Degree Examination, Dec. 2018/Jan. 2019
(CBCS Scheme)
ELECTRONICS
(Digital System Design)

Time : 3 Hours   Max. Marks : 70

PART – A

Answer **all** questions.   **(2×5=10)**

1. a) Compare STATIC RAM with DYNAMIC RAM.

   b) List advantages of CMOS.

   c) What is a prime implicant ?

   d) Simplify using Karnaugh map $f(x, y, z) = \Sigma\, m(2, 3, 5, 7)$.

   e) Minimise the Boolean function $f = xy + \overline{x}z + yz$.

PART – B

Note : Answer the following :   **(20×3=60)**

2. a) Minimize the following using Tabular method.

   $F(A, B, C, D) = \Sigma\, m(4, 5, 6, 8, 10, 13)$.   **10**

   b) Design a mod-5 asynchronous counter.   **10**

   OR

3. a) Design a mod-5 synchronous counter.   **10**

   b) Minimize the following using Karnaugh map.

   $F(A, B, C, D) = \Sigma\, m(4, 5, 6, 8, 10, 13)$.   **10**

4. a) Explain the difference between PAL, PLA and PROM in detail. **10**

   b) Draw the PLA block diagram and explain its operation with example. **10**

   OR

5. a) What is race around condition and how can you solve it in JK ? **10**

   b) Write the circuit diagram for four bit Parallel in Parallel out shift register. **10**

6. a) Using an 8 to 1 multiplexer, design a logic circuit to realize the following Boolean function $F(A, B, C) = \Sigma\, m(1, 2, 4)$.

   b) Using two 2 to 4 decoders, design a logic circuit to realize the following Boolean function $F(A, B, C) = \Sigma\, m(0, 1, 4, 6, 7)$. **(10+10)**

   OR

7. a) Explain different logic families and compare them.

   b) What are the advantages of CMOS logic and explain their electrical behavior with timing diagram and circuit. **(10+10)**

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